



**CSET 112 Computer Organization  
Second Semester 2009 (082)**

2009 Catalog Description: (2 2 3) CSET 112: is a course that teaches the basic structure of computer hardware and software. This course covers the architecture of processor, memory and cache design principles, pipelining principles, addressing modes and instruction design parameters, interrupt driven systems, and assembly language. It focuses on the processing unit design and operation using selected examples. Performance of different computer hardware components and performance enhancement is considered. This course is offered for freshmen majoring in computer technology.

**Prerequisites:** None

<b>Textbook</b>	▪	L. Null & J. Labur, Comp. Organization & Architecture, Jones & Bartlett Publishers 2003 (TB)	
<b>Laboratory manuals</b>	▪	HBCC, CSET-112 manuals	(LM)
<b>Notes</b>	▪	HBCC, CSET-112, handouts	(HO)
<b>Coordinator</b>	▪	Dr. Lawan Ahmad Mohammad.	
<b>Instructor</b>	▪	Dr. Mubarak Al-Mutairi	

**Goals:** The purpose of this course is to introduce fundamental concept of computer devices organization and operation. Provide students with the details of program sequencing and execution. Introduce students to the basics of computer hardware components and have the students skillfully perform laboratory experiments to get use to these components. Provide students with the basic principles of machine programming and assembly language.

**Topics:**

1. Introduction to computers (2 hours)
2. Structured layers of a computer system (2 hours)
3. Number systems (4 hours)
4. Central processing unit organization (4 hours)
5. Instruction sets and addressing modes (4 hours)
6. Main memory organization (6 hours)
7. Secondary storage organization (2 hours)
8. Input/Output Devices Interaction/organization (2 hours)
9. Computer communications (4 hours)

**Weekly schedule:** attached.

**Assessment Policy:**

**Weighting:**

**Letter Grading Scale:**

Quizzes	05%	00.0% < 60.0%	= F
Home work	05%	60.1% < 65.0%	= D
Lab Quizzes	05%	65.1% < 70.0%	= D+
Lab Mid-term Exam	10%	70.1% < 75.0%	= C
Lab Final Exam	10%	75.1% < 80.0%	= C+
First Major exam	15%	80.1% < 85.0%	= B
Second Major Exam	15%	85.1% < 90.0%	= B+
Project	05%	90.1% < 95.0%	= A
Final Exam	30%	95.1% to 100%	= A+

Some clustering and adjustment of threshold values may be applied depending on final results statistics of discreet groups.

**HBCC Rules and Regulations:**

1. **Attendance:** students are expected to attend all meeting of their courses. In the case of any absence, students are responsible for course content during their absence.
2. **Absenteeism:** a record is consistently compiled and updated. If the student has been absent too many times without a valid excuse, he will be excluded from the college.
3. **Smoke free college:** smoking is prohibited in all college facilities.
4. **Behavior:** students who engage in behavior that disrupts the learning environment for others may be subjected to disciplinary action under the KFUPM code.
5. **Exam cheating:** it is not permitted to speak during the exam. Failure to abide by this rule will result in their exam marks being cancelled.

**Prepared By:** Dr. Mubarak Al-Mutairi

**Signature:** \_\_\_\_\_

**Date:** \_\_\_\_\_

**Prepared By:** Dr. Hamza Maghraby

**Signature:** \_\_\_\_\_

**Date:** \_\_\_\_\_



Week no.	Contents	Handout no. & Text Ref.	Practical / Support activities	Assessment
1	Functional units organization. Bus structure and performance.	TB: Sections 1.1-1.3 (1-10)		
2	Software, performance. Distributed computing.	TB: Sections 1.4-1.6 (10-16)	Exercise # 1 PC Components	Quiz # 1
3	Addressing methods and machine program sequencing.	TB: Sections 2.1- 2.4 (21- 40)	Exercise # 2 Motherboard assembling	HW # 1
4	Input-output organization, basic operational techniques. Accessing I/O devices and interrupts.	TB: Sections 2.6, 4.1, 4.2 (47, 152-169)	Exercise # 3 Motherboard reassembling	Quiz # 2
5	Direct memory access. I/O hardware, standard I/O interface.	TB: Sections 4.4- 4.7 (175- 201)	Exercise # 4 I/O assembling & reassembling	HW # 2
<b>MAJOR-1 EXAM (During week 6)</b>				
6	Memories types, semiconductor RAM design and operation. ROM, memory speed, size, and cost.	TB: Sections 5.1- 5.4 (207- 226)	Exercise # 5 Power supply assembling	Quiz # 3
7	Cache memories concepts. Virtual memories and memory management requirements.	TB: Sections 5.5 - 5.9 (226 – 252)	Exercise # 6 Power supply reassembling	HW # 3
8	Microprocessor design and fundamental concepts.	TB: Section 3.1 (111-118)	Practical Exam on PC assembling & reassembling	Lab Mid-Term Exam
<b>Lab Mid-term EXAM (During week 8)</b>				
9	Execution of a complete instruction. Hardwired control organization and operation.	TB: Sections 3.2 and 3.3 (118-126)	Students activities (Presentations & active sessions)	Quiz # 4
10	Performance considerations. Micro programmed control organization and operation.	TB: Sections 3.4 – 3.6 (126-146)	Students activities (Presentations & active sessions)	HW # 4
<b>MAJOR-2 EXAM (During week 11)</b>				
11	Assembly language.	TB: Section 2.5 (41- 46)	Assembly programming basic concepts	
12	Assembly language.	Handouts No. 1	Programming exercise # 1	Quiz # 5
13	Assembly language.	Handouts No. 2	Programming exercise # 2	HW # 5
14	Assembly language.	Handouts No. 3	Programming exercise # 3	
<b>Lab Final EXAM (During week 15)</b>				
15		Revision	Lab Final Exam	
<b>Final Examination (week 16)</b>				

- NB:** Major-I exam will be conducted in 6<sup>th</sup> week.  
Major-II exam will be conducted in 11<sup>th</sup> week.  
Lab Project must be submitted in 15<sup>th</sup> week.  
Final exam will be conducted in 16<sup>th</sup> week.  
Necessary handouts will be provided.